MEMORY DEVICE HAVING MULTIPLE ARRAY STRUCTURE FOR INCREASED BANDWIDTH

Abstract

One embodiment of the present invention provides a semiconductor memory including a bank of N memory arrays each having a corresponding array address, a bus providing an array address signal, a row address signal (RAS), and timing signals. The semiconductor memory further includes N tracking circuits each coupled between a different one of the N memory arrays and the bus. A first tracking circuit, in response to receiving a first array address for a first array via the array address signal and a first active state of the RAS, couples the first array to the bus such that only the first array responds to a first sequence of timing signals constituting a first bank transaction. A second tracking circuit, in response to receiving a second array address for a second array via the array address signal and a second active state of the RAS, couples the second array to the bus such that only the second array begins responding to second sequence of timing signals constituting a second bank transaction before the first bank transaction is complete.